A METHOD TO AVOID THRESHOLD VOLTAGE SHIFT IN THICKER DIELECTRIC FILMS

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Background of the Invention

1.   Field of the Invention

This invention relates to integrated circuit structures, and in particular, it relates to dielectric materials used within dynamic random access memory cells formed on semiconductor integrated circuits.

2.   Background Art

In a conventional transistor a gate is separated from the source and drain by a dielectric layer.   When a sufficient voltage level is applied to the gate the transistor turns on and current flows between the source and the drain of the transistor.   In a similar manner, when conductors of integrated

circuits pass over dielectric layers located above adjacent n-wells or diffusion regions they can cause leakage current to flow between the n-wells or between the diffusion regions. This leakage current is very undesirable.

It is well known in the art of semiconductor fabrication that dielectric layers formed from organic sources can have shifts in their threshold voltage due to impurities in the dielectric material. The impurities are present in the layer because of the organic processes, such as ozone-TEOS based chemistry, which are used to form the material of the dielectric layer.

It is also known for the impurities in the dielectric layer to diffuse and collect at interfaces close to the substrate during high temperature processing steps performed after deposition of dielectric material formed with organometallic precursors. This diffusion can seriously degrade integrated circuit operation.

It is therefore an object of the present invention to provide a process for forming dielectric material for semiconductor fabrication using organic chemistry such as ozone-TEOS based chemistry and organometallic precursors which leave undesirable impurities in the dielectric material.

It is a further object of the present invention to eliminate or reduce threshold voltage shift caused by impurities that are a consequence of the organic processes for forming the dielectric layer.

It is a further object of the present invention to provide such a process for BPSG films that are thicker than at least 5KA.

It is a further object of the present invention to prevent the problems associated with diffusion of impurities in dielectric layers to interfaces near the surface of the substrate.

These and other objects and advantages of the invention will become more fully apparent from the description and claims which follow or may be learned by the practice of the invention.

Summary of the Invention

A method of fabricating an integrated circuit having reduced threshold voltage shift is provided. A nonconducting region is formed on the semiconductor substrate and active regions are formed on the semiconductor substrate. The active regions are separated by the nonconducting region. A barrier layer and a dielectric layer are deposited over the nonconducting region and over the active regions. Heat is applied to the integrated circuit causing the barrier layer to anneal. The dielectric layer can be a BPSG film. Preferably BPSG films are deposited using organometallic precursors. More specifically, ozone (4 to 20% vol conc.), TEOS, TEPO (as an example of a P source) and TEB (as an example of a B source) are reacted at a temperature of at least 300°C such that BPSG films of at least one thousand angstroms are formed at a deposition rate in the range of 500 angstroms/min to 6000 angstroms/min using gas or liquid injection for carrying the species into the reaction

chamber. The preferred deposition temperature range is 300°C - 600°C. The deposition may be done at atmospheric or subatmospheric pressure, in a plasma or a non-plasma based reactor and deposition conditions and the dopant concentration can be varied to obtain the desired film properties and composition. Hot wall reactors can also be used for BPSG film deposition.

Brief Description of the Drawings

In order that the manner in which the above-recited and other advantages and objects of the invention are obtained can be appreciated, a more particular description of the invention briefly described above will be rendered by reference to a specific embodiment thereof which is illustrated in the appended drawings. Understanding that these drawings depict only a typical embodiment of the invention and are not therefore to be considered limiting of its scope, the invention and the presently understood best mode thereof are described and explained with additional specificity and detail through the use of the accompanying drawings.

Fig. 1 shows a cross-sectional schematic representation of a prior art semiconductor integrated circuit which may be used in accordance with the method of the present invention.

Fig. 2 shows a graphical representation of the threshold voltage shift in integrated circuits that is solved by the method of the present invention.

Fig. 3 shows a cross-sectional schematic representation of the semiconductor integrated circuit of Fig. 1 including a barrier layer formed in accordance with the method and structure of the present invention.

Detailed Description of the Invention

Referring now to Fig. 1, there is shown a prior art cross-sectional representation of a semiconductor device 10. Active regions 12 are formed within a silicon layer 18. It will be understood by those skilled in the art that the active regions 12 can be any type of diffused regions such as n+, p+, n-, or p- regions or collections of transistors formed within n-wells or p-wells. The active regions 12 are separated from each other by an insulating region 14. It will also be understood by those skilled in the art that the insulating region 14 spacing the active regions apart may be, for example, a field oxide region between two diffusion regions, a trench oxide or any other type of isolating region. Thus, region 14 can be any kind of insulating region between active areas within an n-well or a p-well. A dielectric layer 20 is deposited over the active regions 12 and the field oxide layer 14. The dielectric layer 20 can be formed of, for example, BPSG, BSG, PSG or silicon dioxide. A lead 26 is located above the dielectric layer 20. During use of an integrated circuit formed with the semiconductor device 10 a voltage level on the lead 26 may give rise to a small leakage current 16 between the active regions 12 under the insulating region 14.

Leakage current 16 between isolated active areas in a p-well or an n-well is enhanced by the presence of oxide charges 24 within the dielectric layer 20 upon application of a voltage to lead 26. While oxide charges 24 are indicated with "+" in the drawings for illustrative purposes, it will be understood that oxide charges 24 can be positive or negative. For example, negative charges can be present with an n-well structure and positive charges can be present with a p-well structure. Thus, the leakage current between active areas in an n-well structure is enhanced by the presence of negative oxide charges. If additional oxide charges 24 are present in the dielectric layer 20 the problems associated with oxide charges 24 increase. Thus, when the dielectric layer 20 is formed with a greater thickness, the problems are increased due to the greater amount of oxide charges 24 that are carried by the additional BPSG or other material of the thicker dielectric layer 20. The oxide charges 24 are a substantial problem for thicknesses over one thousand angstroms.

Referring now to Fig. 2, there is shown a graphical representation 50 for a p-type substrate 18. The graphical representation 50 illustrates the relationship between the voltage applied to the lead 26 and the capacitance in the dielectric layer 20. If there is no oxide charge 24 in the dielectric layer 20 the curve 54 results. If positive charges 24 are present in the dielectric layer 20 the flatband shift of curve 52 results. If negative charges 24 are present in the dielectric layer 20 the flatband shift of curve 56 results.

The primary source of the oxide charges 24 present within the dielectric layer 20 is contamination of the dielectric layer 20. One of the potential sources of the contamination in the dielectric layer 20 can be carbon. The contamination of the layer 20 occurs during production of the BPSG or other type of material forming layer 20. It is well understood that molecules acting as sources of boron, phosphorous and silicon atoms must react with oxygen in order to form the BPSG, BSG, PSG or other material of the dielectric layer 20. The contamination of the dielectric layer 20 can thus occur due to the use of organometallic precursors that can be used to provide the boron, phosphorus, silicon and oxygen atoms of the BPSG of the dielectric layer 20.

For example it is known to form the BPSG material of the dielectric layer 20 by reacting ozone with organic precursors such as $(C_2H_5O)_4Si$ (TEOS) triethylphosphate ~~tetraethylorthophosphate~~ (TEPO) and triethylborane (TEB) in order to provide the required boron, phosphorous, and silicon atoms. Each of these molecules is an organic molecule containing carbon atoms. The contamination due to the carbon of the organic molecules remains in the BPSG dielectric layer 20 after the reactions forming the BPSG material and cause impurities in the BPSG layer 20. Furthermore, it will be understood that contamination can arise in any other way from the organic precursors and from any other sources. For example, impurities mixed with the organic precursors can cause the contamination. The contamination causes the oxide charges 24 to be present

in the dielectric layer 20 and, thereby, causes threshold voltage shift. Other contamination sources can also be present that would give rise to charged regions in oxide.

5   It is also known in the prior art to obtain the boron, phosphorus and silicon atoms required for forming the BPSG or other material of the dielectric layer 20 from sources that are not organic sources and do not contaminate the layer 20 in this manner. For 10   example, either in the presence of a plasma or at atmospheric pressure, oxygen may be reacted with silane (SiH_4), phosphine (PH_3) and/or diborane (B_2H_6) in order to form BPSG.

However, the use of organometallic precursors such as TEOS, TEPO and TEB to form dielectric materials 15   for semiconductor fabrication is preferred to the use of the inorganic materials for several reasons. The organic reactions permit better control of the fabrication process. For example, the organic 20   reactions provide more precise control of doping and oxide thickness. Furthermore, they permit better step coverage.

Referring now to Fig. 3, there is shown a cross-sectional representation of a semiconductor 25   device 100 formed in accordance with a preferred method of the present invention. The semiconductor device 100 is substantially similar to the semiconductor device 10 except for the addition of a barrier layer 30. The barrier layer 30, is deposited below the dielectric 30   layer 20 and above the active regions 12 and the insulating region 14.

The depositing of layer 20 can be followed by heating the layer 20 to at least 550°C. In one preferred embodiment rapid thermal processing is performed. In rapid thermal processing, the temperature of layers 20 and 30 is raised to between approximately 850°C and 1050°C for at least five seconds causing the layer 20 to reflow. In another preferred embodiment the temperature can be raised to approximately 750°C to 1000°C in a furnace for at least five minutes. During the reflow of the dielectric layer 20, and during any other subsequent high temperature process steps which may occur, the impurities within the dielectric layer 20 may diffuse. For example, without the barrier layer 30 the impurities may diffuse to the interface between the dielectric layer 20 and the active regions 12 and, more likely, to the interface between the dielectric layer 20 and the insulating region 14 and degrade the performance of the integrated circuit. The barrier layer 30 blocks diffusion of the impurities into the active regions 12 and into the insulating region 14 during the reflow step and/or any other high temperature process steps.

The barrier layer 30 can be formed in many different ways. For example, the barrier layer 30 can be a silane-based oxide layer or a silane-based oxynitride layer. Additionally, the barrier layer 30 can be a nitride film which can be formed using plasma technology or using non-plasma technology. Additionally, a silane-based nitride or nitride with a silane-based oxide stack can be used. Additionally, the layer 30 can be a composite layer formed of layers of silicon dioxide and silicon nitride. Thus, in accordance with the present invention the organic dielectric layer 20 is deposited

over any of these barrier layers 30 or barrier stacks 30. The barrier layer 30 formed in this manner can be in the range of approximately fifty angstroms to approximately two thousand angstroms. Preferably, it is between one-hundred and one-thousand angstroms.

Prior to depositing the barrier layer 30 and before forming any of the previously described stacks a plasma treatment of the semiconductor device 10 can be performed. The plasma treatment can be a conventional high voltage plasma treatment using oxygen plasma, ozone plasma, nitrogen plasma, ammonia plasma or a combination of the these gases.

It has been determined that the refractive index of materials can serve as an indication of whether they are suitable for forming the material of the barrier layer 30 of the present invention because the index of refraction of these materials is related to their nitrogen content. The range of satisfactory refractive indices for a material to function as the barrier layer 30 of the present invention is from approximately 1.5 to 2.6. The refractive index of silicon nitride is typically approximately 2.0. The refractive index of oxynitride is typically between approximately 1.46 and 2.0. The refractive index of silicon rich oxynitride is between approximately 2.0 and 2.6. The refractive index of silicon dioxide is approximately 1.46. The refractive index of a composite layer 30 formed of silicon dioxide and silicon nitride is somewhere between the indices of the silicon dioxide and silicon nitride depending on the relative amount of each material used in forming the layer. Although other barrier materials having a refractive index within the range can be used, it will

be understood that a material forming the barrier layer 30 must be structurally sound in addition to having a refractive index in this range. It is thus understood that many other materials can be used to form the layer 30. For example, aluminum oxide and aluminum nitride and other insulating materials can be used.

It is to be understood that although the present invention has been described with reference to a preferred embodiment, various modifications, known to those skilled in the art, may be made to the structures and process steps presented herein without departing from the invention as recited in the several claims appended hereto. For example, the use of the barrier layer 30 is taught under the lead 26 and over the active regions 12 and the insulating region 14. In one preferred embodiment, the barrier layer 30 of the present invention may be deposited above n-wells and/or p-wells wherein integrated circuit active regions are formed in the n-wells and/or p-wells in a conventional manner. It will be understood that the method of the present invention prevents n-well to n-well leakage and p-well to p-well leakage as well as preventing leakage between active regions within n-wells or p-wells. Furthermore, the method of the present invention may be used to prevent metal field leakage and poly field leakage in general.